## Claims

[c1] What is claimed is:

1. A reader for use with a tag that communicates data to the reader, the reader comprising:

a coil;

at least one capacitor;

A a means for coupling the capacitor(s) to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-means signal(s), the coupling means being a transformer;

B a means for driving the coil through the capacitor(s) with a driving signal;

C a means for generating the driving signal;

D a means for extracting the data communicated by the tag from a coupling-means signal.

[c2] 2. The reader of claim 1 wherein the coupling means is a transformer having a first winding and a second winding, the capacitor(s) being connected to the first winding, the coil being connected to the second winding, and the data-extracting means being connected to the first winding.

[c3] 3. The reader of claim 1 wherein the coupling means is a transformer having a first winding and a second winding, the capacitor(s) being connected to the first winding, the coil being connected to the second winding, and the data-extracting means being connected to the second winding.

[c4] 4. The reader of claim 1 wherein the coupling means is a transformer having a first winding, a second winding, and a third winding, the capacitor(s) being connected to the first winding, the coil being connected to the second winding, and the data-extracting means being connected to the third winding.

[c5] 5. A reader for use with a tag, the reader comprising:

a coil;

at least one capacitor;

a means for coupling the capacitor(s) to the coil;

a means for driving the coil through the capacitor(s) with a driving signal;

a means for generating the driving signal;

a means for embedding a bit-timing clock signal in the driving signal;

a means for embedding a sequence of bits to be communicated to a tag in the driving signal.

[c6] 6. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted.

[c7] 7. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

[c8] 8. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

[c9] 9. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

[c10] 10. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted.

[c11] 11. The reader of claim 5 wherein the means for embedding a sequence of bits

comprises:

a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

[c12] 12.The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

[c13] 13. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

[c14] 14. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for causing the phase of the driving signal (1) to have a first phase and a first frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted.

[c15] 15. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:

a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

[c16] 16. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:
a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

[c17] 17. The reader of claim 5 wherein the means for embedding a sequence of bits comprises:
a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

[c18] 18. The reader of claim 5 wherein the bit-timing clock signal is used by the tag to control the start time of each bit transmitted to the reader, the reader further comprising:
a means for extracting data communicated by the tag from a coupling-means signal.

[c19] 19. The reader of claim 18 wherein the tag transmits a first signal during a bit period when a "0" bit is to be communicated and a second signal during a bit period when a "1" is to be communicated, the data-extracting means comprising:
a means for identifying the bit communicated by the tag during each bit period, the start of each bit period being determined by the bit-timing clock signal.

[c20] 20. The reader of claim of 19 wherein the bit identifying means comprises:
a means for obtaining at least one weighted integration of the coupling-means signal;
a means for translating the weighted integration(s) into a bit value.

[c21] 21. The reader of claim of 19 wherein the bit identifying means comprises:
a means for obtaining at least one weighted integration of the amplitude of the coupling-means signal;
a means for translating the weighted integration(s) into a bit value.

[c22] 22. The reader of claim of 19 wherein the bit identifying means comprises:
a means for obtaining at least one weighted integration of the phase of the coupling-means signal;
a means for translating the weighted integration(s) into a bit value.

[c23] 23. The reader of claim 19 wherein the first signal is a periodic signal with a first value for a predetermined signal parameter and the second signal is the periodic signal with a second value for the predetermined signal parameter, the predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the bit-identifying means comprising:
a means for generating a first replica of the periodic signal with the first value for the predetermined signal parameter and a second replica of the periodic signal with the second value for the predetermined signal parameter;
a means for multiplying the coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;
a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

[c24] 24. The reader of claim 19 wherein the first signal is a periodic signal with a first value for a first predetermined signal parameter and the second signal is the periodic signal with a second value for the first predetermined signal parameter, the first predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the periodic signal modulating a second predetermined signal parameter of a carrier signal, the second predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the carrier signal, the bit-identifying means comprising:

a means for demodulating the second predetermined signal parameter of the coupling-means signal;
a means for generating a first replica of the periodic signal with the first value for the first predetermined signal parameter and a second replica of the periodic signal with the second value for the first predetermined signal parameter;
a means for multiplying the demodulated coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;
a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

[c25] 25. A reader for use with a tag that transmits a periodic signal having a first frequency when a "0" bit is to be communicated and a second frequency when a "1" bit is to be communicated, the reader comprising:
a means for receiving the tag signal;
a means for measuring the period of each cycle of the signal received from the tag during a bit period.

[c26] 26. The reader of claim 25 further comprising:
a means for identifying the bit transmitted by the tag from the measurements of the period of each cycle of the signal received from the tag during a bit period.

[c27] 27. The reader of claim 26 wherein the means for identifying the bit transmitted by the tag comprises:
a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the absolute value of the difference between the period of the cycle and the period of the first-frequency signal is less than a first predetermined value, the frequency of a cycle being the second frequency if the absolute value of the difference between the period of the cycle and the period of the second-frequency signal is less than a second predetermined value;
a means for identifying the bit transmitted during a bit period from the frequencies of the cycles of the received signal, the bit being a "0" if the number

of first-frequency cycles exceeds the number of second-frequency cycles in the bit period, the bit otherwise being a "1".

[c28] 28. The reader of claim 26 wherein the means for identifying the bit transmitted by the tag comprises:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the period of the cycle is greater than a first predetermined value and less than a second predetermined value, the frequency of a cycle being the second frequency if the period of the cycle is greater than a third predetermined value and less than a fourth predetermined value;

a means for identifying the bit transmitted during a bit period from the frequencies of the cycles of the received signal, the bit being a "0" if the number of first-frequency cycles exceeds the number of second-frequency cycles in the bit period, the bit otherwise being a "1".

[c29] 29. The reader of claim 25 further comprising:

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change greater than a predetermined value in the period of a cycle from one cycle to the next cycle.

[c30] 30. The reader of claim 25 further comprising:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the absolute value of the difference between the period of the cycle and the period of the first-frequency signal is less than a first predetermined value, the frequency of a cycle being the second frequency if the absolute value of the difference between the period of the cycle and the period of the second-frequency signal is less than a second predetermined value;

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change in frequency from one cycle to the next.

[c31] 31. The reader of claim 25 further comprising:

a means for identifying the frequency of each cycle of the received signal, the frequency of a cycle being the first frequency if the period of the cycle is greater

than a first predetermined value and less than a second predetermined value, the frequency of a cycle being the second frequency if the period of the cycle is greater than a third predetermined value and less than a fourth predetermined value;

a means for identifying the beginning of a bit period, the beginning of a bit period being identified by a change in frequency from one cycle to the next.

[c32] 32. A reader for use with a tag that communicates data to the reader by repeating a message a plurality of times, the message comprising a preamble consisting of a sync sequence of S bits, a tag data group of T bits, and an error-detecting group of E bits, the data group and the error-detecting group including false-sync sequences, the reader comprising:

a means for receiving the data sequence transmitted by the tag;

a means for detecting each sync sequence in the received data sequence;

a means for identifying the preamble;

a means for extracting the tag data from the received data sequence utilizing the identification of the preamble.

[c33] 33. The reader of claim 32 wherein the preamble identifying means comprises:

a means for detecting errors in the T + E bits following each detected sync sequence assuming that the sequence in question is the preamble, the presence of errors indicating that the sync sequence in question is a false-sync sequence, the absence of errors indicating that the sequence is, in fact, the preamble.

[c34] 34. The reader of claim 33 wherein the sync sequence detecting means comprises:

a memory for storing (S+T+E) received data bits;

a means for determining whether the oldest S bits in memory is a sync sequence;

a means for replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits;

a control means for causing the determining means and the replacing means to operate alternately after the memory is filled with received bits.

[c35] 35. The reader of claim 33 wherein the sync sequence detecting means

comprises:

a memory for storing (S+T+E) received data bits;

a first means for determining whether the newest S bits in memory is a sync sequence;

a second means for determining whether the oldest S bits in memory is a sync sequence;

a means for replacing the oldest bit in memory with the next received bit after the memory has been filled with received bits;

a control means for causing the first determining means and the replacing means to operate alternately until a sync sequence is detected, the control means causing the second determining means and the replacing means to operate alternately if a detected sync sequence is determined to be a false-sync sequence.

[c36] 36. A reader for use with a tag, the reader comprising:

a coil;

at least one capacitor;

a means for coupling the capacitor(s) to the coil;

a means for driving the coil through the capacitor(s) with a driving signal, the means consisting of four field-effect transistors connected in a bridge arrangement, two opposing junctions being connected to a power supply, the driving signal being available at the remaining two opposing junctions, the current flow through the transistors being controlled by a control signal applied to the gate of each transistor;

a means for generating at least one control signal.

[c37] 37. The reader of claim 36 wherein the bridge circuit comprises two series-connected P- and N-channel field effect transistors connected in parallel, the junction of the P devices and the junction of the N devices being connected to a voltage supply, the driving signal being available at the junctions of the P and N devices.

[c38] 38. The reader of claim 37 further comprising:

a diode connected between gate and source of each transistor to protect the

gates from voltage spikes;

a resistor in series with each gate of each transistor to suppress ringing in the gate circuit when the transistor is turned on.

[c39] 39. The reader of claim 36 wherein the bridge circuit comprises four N-channel field effect transistors connected source to drain, source to source, drain to source, and drain to drain, the junction of the drains and the junction of the sources being connected to a voltage supply, the driving signal being available at the source-drain junctions.

[c40] 40. The reader of claim 39 further comprising a two-winding transformer associated with each transistor, a control signal being fed into one winding of a transformer, the other winding being connected between gate and source electrodes of the associated transistor.

[c41] 41. A tag for use with a reader, the tag comprising:

a coil;

a capacitor;

a means for driving the coil;

a means for coupling the capacitor and the driver to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-means signal(s), the coupling means being a transformer;

a means for extracting the data communicated by the reader from a coupling-means signal;

a means for extracting power from the coupling-means signal to operate the tag.

[c42] 42. The tag of claim 41 wherein the coupling means is a transformer having a first winding and a second winding, the capacitor, the driving means, the data-extraction means, and the power-extraction means being connected to the first winding, the coil being connected to the second winding.

[c43] 43. The tag of claim 41 wherein the coupling means is a transformer having a first winding and a second winding, the capacitor and the driving means being

connected to the first winding, the coil, the data-extraction means, and the power-extraction means being connected to the second winding.

[c44] 44. The tag of claim 41 wherein the coupling means is a transformer having a first winding, a second winding, and a third winding, the capacitor and the driving means being connected to the first winding, the data-extraction means and the power-extraction means being connected to the second winding, and the coil being connected to the third winding.

[c45] 45. The tag of claim 41 wherein the coupling means is a transformer having a first winding, a second winding, a third winding, and a fourth winding, the capacitor and the driving means being connected to the first winding, the data-extraction means being connected to the second winding, the power-extraction means being connected to the third winding, and the coil being connected to the fourth winding.

[c46] 46.The tag of claim 41 wherein the coupling means is a transformer having a first winding, a second winding, a third winding, a fourth winding, and a fifth winding, the capacitor being connected to the first winding, the driving means being connected to the second winding, the data-extraction means being connected to the third winding, the power-extraction means being connected to the fourth winding, and the coil being connected to the fifth winding.

[c47] 47. A tag for use with a reader, the reader communicating a sequence of bits to the tag by transmitting a first signal during a bit period when a "0" bit is to be communicated and a second signal during a bit period when a "1" is to be communicated, the reader embedding a bit-timing clock signal in the transmitted signals, the tag comprising:

a coil;

a capacitor;

a means for coupling the capacitor to the coil and coupling the coil to at least one other means, the signal(s) provided to the other means as a result of the coupling being called coupling-means signal(s), the combination of the coil, the capacitor, and the coupling means being called the resonating circuit;

a means for generating a bit-timing clock signal that is synchronized to the bit-

timing clock signal embedded in the transmitted signals;

a means for identifying the bit being transmitted during each bit period, the beginning and ending of each bit period being indicated by the bit-timing clock signal.

[c48] 48. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the coupling-means signal; weight of "1"

a means for translating the weighted integration(s) into a bit value.

[c49] 49. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the amplitude of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

[c50] 50. The tag of claim of 47 wherein the bit identifying means comprises:

a means for obtaining at least one weighted integration of the phase of the coupling-means signal;

a means for translating the weighted integration(s) into a bit value.

[c51] 51. The tag of claim 47 wherein the first signal is a periodic signal with a first value for a predetermined signal parameter and the second signal is the periodic signal with a second value for the predetermined signal parameter, the predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the bit-identifying means comprising:

a means for generating a first replica of the periodic signal with the first value for the predetermined signal parameter and a second replica of the periodic signal with the second value for the predetermined signal parameter;

a means for multiplying the coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

[c52] 52. The reader of claim 47 wherein the first signal is a periodic signal with a first value for a first predetermined signal parameter and the second signal is the periodic signal with a second value for the first predetermined signal parameter, the first predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the periodic signal, the periodic signal modulating a second predetermined signal parameter of a carrier signal, the second predetermined signal parameter being one of the signal parameters amplitude, phase, and frequency that characterize the carrier signal, the bit-identifying means comprising:

a means for demodulating the second predetermined signal parameter of the coupling-means signal;

a means for generating a first replica of the periodic signal with the first value for the first predetermined signal parameter and a second replica of the periodic signal with the second value for the first predetermined signal parameter;

a means for multiplying the demodulated coupling-means signal by the first replica thereby obtaining a first product waveform and by the second replica thereby obtaining a second product waveform;

a means for integrating the first and second product waveforms for a bit period and translating the integration results into a bit value.

[c53] 53. The tag of claim 47 wherein the bit-identifying means comprises:

a means for generating replicas of the first and second signals transmitted by the reader;

a means for obtaining the amplitude of a coupling-means signal as a function of time;

a means for multiplying the coupling-means signal amplitude by the replica of the first signal to obtain a first product signal and by the replica of the second signal to obtain a second product signal;

a means for integrating the first product signal over a bit period to obtain a first integration and integrating the second product signal over a bit period to obtain a second integration;

a means for translating the first and second integrations into a bit value.

[c54] 54. The tag of claim 47 wherein the means for generating a bit-timing clock signal that indicates the start of each bit period comprises:
a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;
a means for recognizing the bit transition in the coupling-means signal from one bit to the next;
a means for adjusting the bit-start indicators until the bit-start indicators and the bit transitions in the coupling-means signal occur simultaneously.

[c55] 55. The tag of claim 47 wherein the reader embeds a bit-timing clock signal in the transmitted signals by initially alternating the transmission of the first signal and the second signal, the means for generating a bit-timing clock signal that indicates the start of each bit period comprising:
a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;
a means for recognizing the bit transitions in the coupling-means signal resulting from the transitions from the first signal to the second signal and from the second signal to the first signal;
a means for adjusting the bit-start indicators until the bit-start indicators and the transitions in the coupling-means signal occur simultaneously.

[c56] 56. A tag for use with a reader, the reader transmitting a bit-timing clock signal to the tag, the tag comprising:
a coil;
a capacitor;
a means for coupling the capacitor to the coil;
a means for driving the coil with a driving signal;
a means for generating the driving signal;
a means for generating a bit-timing clock signal synchronized to the reader bit-timing clock signal;
a means for embedding a sequence of bits to be communicated to a reader in the driving signal, the start of each bit being controlled by the bit-timing clock signal.

[c57] 57. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for causing the phase of the driving signal to have a first phase when a "0" bit is being transmitted and to have a second phase when a "1" bit is being transmitted.

[c58] 58. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for modulating the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

[c59] 59. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for modulating the amplitude of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

[c60] 60. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for modulating the phase of the driving signal with a periodic signal having a first phase when a "0" bit is being transmitted and having a second phase when a "1" bit is being transmitted.

[c61] 61. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for causing the phase of the driving signal to have a first frequency when a "0" bit is being transmitted and to have a second frequency when a "1" bit is being transmitted.

[c62] 62. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for modulating the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

[c63] 63. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for modulating the amplitude of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

[c64] 64. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for modulating the phase of the driving signal with a periodic signal having a first frequency when a "0" bit is being transmitted and having a second frequency when a "1" bit is being transmitted.

[c65] 65. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for causing the phase of the driving signal (1) to have a first phase and a first frequency when a "00" bit pair is being transmitted, (2) to have a first phase and a second frequency when a "01" bit pair is being transmitted, (3) to have a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) to have a second phase and a second frequency when a "11" bit pair is being transmitted.

[c66] 66. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for modulating the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

[c67] 67. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for modulating the amplitude of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair

is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

[c68] 68. The tag of claim 56 wherein the means for embedding a sequence of bits comprises:
a means for modulating the phase of the driving signal with a periodic signal (1) having a first phase and a first frequency when a "00" bit pair is being transmitted, (2) having a first phase and a second frequency when a "01" bit pair is being transmitted, (3) having a second phase and a first frequency when a "10" bit pair is being transmitted, and (4) having a second phase and a second frequency when a "11" bit pair is being transmitted.

[c69] 69. The tag of claim 56 wherein the reader transmits the bit-timing clock signal to the tag by communicating a sequence of alternating "0" and "1" bits, a "0" bit being communicated by modulating the amplitude of the driving signal with a first periodic signal, a "1" bit being communicated by modulating the amplitude of the alternating field with a second periodic signal, the means for generating the clock signal that is synchronized to the bit-timing signal transmitted by the reader to the tag comprising:
a means for generating a clock signal having a bit-start indicator during each bit period, the bit-start indicators being adjustable in time;
a means for obtaining the amplitude of a coupling-means signal as a function of time;
a means for recognizing the transitions in the coupling-means signal amplitude at the time interfaces of the first and second periodic signals;
a means for adjusting the bit-start indicators until the bit-start indicators and the transitions in the coupling-means signal amplitude occur simultaneously.

[c70] 70. A method for interrogating a tag comprising the steps:
generating an alternating magnetic field;
embedding a bit-timing clock signal in the alternating magnetic field;
embedding data to be communicated to a tag in the alternating magnetic field.

[c71] 71. A method for interrogating a tag, the tag responding to an interrogation by

transmitting a sequence of bits, the start of each bit being determined by a bit-timing clock signal generated by the tag and synchronized with a bit-timing clock signal originating with the interrogator, the method comprising the steps:
generating a bit-timing clock signal;
generating an alternating magnetic field in which the bit-timing clock signal is embedded;
extracting data transmitted by the tag utilizing the bit-timing clock signal.

[c72] 72. A method of receiving a communication from a tag which transmits a repeating message comprising a preamble consisting a sync sequence of S bits, a tag data group of T bits, and an error-detecting group of E bits, the data group and the error-detecting group possibly including false-sync sequences, the method comprising the steps:
receiving the data sequence transmitted by the tag;
detecting each sync sequence in the received data sequence;
identifying the preamble;
extracting the tag data from the received data sequence utilizing the identification of the preamble.

[c73] 73. A method for responding to an interrogation by a reader, the method utilizing a resonating circuit comprising at least one capacitor coupled to a coil, the method comprising the steps:
driving the resonating circuit with a driving signal;
maintaining the resonating circuit in resonance;
embedding the sequence of bits to be communicated to the reader in the driving signal.

[c74] 74. A method for responding to the establishment of an alternating magnetic field by a reader, the reader embedding a bit-timing clock signal in the alternating magnetic field and communicating a sequence of bits by modulating the alternating magnetic field, the method comprising the steps:
deriving a signal from the alternating magnetic field;
generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field;

performing at least one weighted integration of the derived signal over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

identifying the bit being transmitted during each bit period utilizing the weighted integration(s).

[c75] 75. A method for responding to the establishment of an alternating magnetic field by a reader, a bit-timing signal being embedded in the alternating magnetic field by the reader, the method comprising the steps:

deriving a signal from the alternating magnetic field;

generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded by the reader in the alternating magnetic field;

generating an alternating magnetic field;

modulating the alternating field generated by the responder with a sequence of bits to be communicated to a reader, the start of each transmitted bit being governed by the bit-timing clock signal.

[c76] 76. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

embedding a bit-timing clock signal in the alternating magnetic field;

extracting data communicated by the responder from an alternating magnetic field generated by the responder;

the method performed by the responder comprising the steps:

extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator;

generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator;

generating an alternating magnetic field;

embedding data to be communicated to the interrogator in the alternating magnetic field generated by the responder, the start of each bit being controlled by the bit-timing clock signal generated by the responder.

[c77] 77. A method of communication between an interrogator and a responder, the

method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

embedding a bit-timing clock signal in the alternating magnetic field;

embedding data to be communicated to the responder in the alternating magnetic field;

the method performed by the responder comprising the steps:

extracting a bit-timing clock signal from the alternating magnetic field generated by the interrogator;

performing at least one weighted integration of a signal derived from the alternating magnetic field generated by the interrogator over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

identifying the bit being transmitted during each bit period utilizing the weighted integration(s).

[c78] 78. An apparatus for practicing the method of claim 73.

[c79] 79. An apparatus for practicing the method of claim 76.

[c80] 80. An apparatus for practicing the method of claim 77.